REMARKS

Claims 1-17, 24, 26 and 32-38 are pending in this application. Claims 18-26 and 27-31 have been withdrawn and subsequently canceled without prejudice or disclaimer. For purposes of expedition, claims 1-2 and 4 have been amended to emphasize on the differences between the "first feedback circuit" and the "second feedback circuit" in order to clearly distinguish over the cited prior art. Claim 14 has been amended to avoid several typographical errors to place in condition for allowance.

Claims 24 and 32-38 has been allowed without the necessity of amendment. Claims 2, 3, 6, 7, 8 and 26 have been conditionally allowed if rewritten in independent form to include all of the limitations of their respective base claims 1 and 4. The Examiner's indication of allowability of these claims is noted with appreciation. However, forbearance is respectfully requested pending Applicants' traversal of the outstanding rejection of base claims 1 and 4.

Claims 1, 4 and 5 have been rejected under 35 U.S.C. §103(b) as being unpatentable over Kardontchik et al., U.S. Patent No. 5,566,204, in view of **newly cited art**, Yeh et al, U.S. Patent No. 5,180,214 as stated on page 2 of the non-final Office Action (Paper No. 12). Separately, claims 1, 4 and 5 have been rejected under 35 U.S.C. §102(b) as being anticipated by Kardontchik et al., U.S. Patent No. 5,566,204, as stated on pages 2-3 of the non-final Office Action (Paper No. 12). However, there is confusion as to which rejection is outstanding and, based on the reasons provided by the Examiner on pages 2-3 of the non-final Office Action (Paper No. 12), the rejection of claims 1, 4 and 5 under 35 U.S.C. §102(b) as being anticipated by Kardontchik et al., U.S. Patent No. 5,566,204, seems unwarranted

and should be withdrawn, particularly, in view of the Examiner's express admission that Kardontchik '204 does **not** disclose the first and second feedback loops [are] integral and proportional controller respectively.

As a result, the only rejection outstanding is the rejection of Applicants' claims 1, 4 and 5 as being unpatentable over Kardontchik et al., U.S. Patent No. 5,566,204, in view of **newly cited art**, Yeh et al, U.S. Patent No. 5,180,214 for reasons stated on pages 2-3 of the non-final Office Action (Paper No. 12). Specifically, the Examiner asserts that Kardontchik '204 discloses all aspects of Applicants' claims 1, 4 and 5, except for "the first and second feedback loops are integral and proportional controller respectively" which is allegedly disclosed by Yeh '214, see FIG. 4, FIG. 6 and 16. However, the Examiner's assertion is factually incorrect. As a result, Applicants respectfully traverse the rejection for reasons discussed herein below.

First of all, base claim 1 defines a phase-locked loop circuit, as shown, for example, in FIG. 1, comprising a phase control unit (2000), a frequency control unit (300) and an oscillator 100; "a first feedback circuit which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and a second feedback circuit which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control, wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously."

Likewise, base claim 4 defines a phase locked loop circuit comprising:

> a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating based on the input signal a second control signal for proportional control of an output signal;

an oscillator responsive to the first and second control signals for outputting a clock signal;

a first feedback circuit for feeding back an output of said oscillator to said oscillator through said first control signal generator unit; and

a second feedback circuit for feeding back the output of said oscillator to said oscillator through said second control signal generator unit,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to operate continuously.

As expressly defined in each of Applicants' base claims 1 and 4, the phase locked loop (PLL) suitable operates such that both the phase control loop (integral control – first feedback circuit) and the frequency control loop (proportional control – second feedback circuit) are always connected and are operating continuously. The frequency control is realized by using F/I conversion to linearize the VCO/CCO characteristic, to thereby realize a wide range operation.

The phase control loop (first feedback circuit) and the frequency control loop (second feedback circuit) are always connected for continuous operation, as shown in FIG. 1, FIG. 2 and described on page 13, lines 19-24 of Applicants' specification. For example, on page 13, lines 19-24, Applicants describe that "the proportional controller 3000 first causes the output signal Sv of oscillator 100 to be synchronized in frequency with the input signal Sin; then, the integral controller 2000 lets the output signal Sv be synchronized in phase with input signal Sin" in order to realize a wide range operation.

In contrast to Applicants' base claims 1 and 4, Kardontchik '204, as a primary reference, only discloses a fast acquisition clock recovery system for high speed

data communications, and more specifically, an integrated CMOS circuit as shown in FIG. 2, including a receiver section with a phase-locked loop (PLL) and a transmitter section with a locked loop (LL), wherein the receiver section provides fast clock acquisition of an incoming data signal. According to Kardonchik '204, the clock recovery scheme utilizes an ordinary timing extraction PLL operation for transceivers in which frequency is made coincident first and then phase is made.

As shown in FIG. 1, the switching between phase information output from the phase detector 54 and frequency information output from the frequency detector 70 is handled by using the MUX 56 in response to the TRANSITION DETECTOR signal 58. Then, the added phase and frequency are passed through the loop filter 60, which constitute an integral-control loop.

However, as clearly seen from FIG. 1 of Kardonchik '204, there are **no** two feedback loops (i.e., first feedback loop and second feedback loop) disclosed anywhere from Kardonchik '204, and the Examiner has **not** addressed these features anywhere in the Office Action (Paper No. 12), used to feedback an output of the oscillator to the oscillator through the phase control unit and the frequency control unit continuously, as currently defined in Applicants' base claims 1 and 4.

As a secondary reference, Yeh '214 does **not** remedy the noted deficiencies of Kardonchik '204 in order to arrive at Applicants' base claims 1 and 4. This is because Yeh '214 discloses a completely different subject matter, specifically, an anti-skid brake control system, as shown in FIG. 2, for use in a fast moving vehicle, such as an aircraft, to stop the vehicle in a short distance while preventing the vehicle from skidding. While a phase-locked loop (PLL) scheme is utilized in the

brake control system, there is **no** connection with Applicants' claimed phase locked-loop circuit arrangement as defined in Applicants' base claims 1 and 4.

Moreover, the Examiner cites FIG. 4, FIG. 6 and FIG. 14 of Yeh '214 for allegedly disclosing that "the first and second feedback loops are integral and proportional controller respectively." However, the citation is misplaced.

In contrast to the Examiner's assertion, FIG. 4 of Yeh '214 illustrates a circuit block diagram of a phase detector, including an up-down counter 34, a D/A converter 33 and a pair of frequency to voltage converters 31, 32. Similarly, FIG. 6 of Yeh '214 illustrates a circuit block diagram of a phase detector and a controller designed for the anti-skid brake control system (ABS). Likewise, FIG. 14 of Yeh '214 illustrates a circuit block diagram of a phase detector and a controller designed for ABS using conventional PLL algorithm. Again, no disclosure of any "the first and second feedback loops are integral and proportional controller respectively" as alleged.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, the Examiner must show that the prior art reference (or references when combined) must teach or suggest all the claim limitations, and that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings, provided with a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not** based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143. In other words, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USQP 494, 496 (CCPA 1970). Moreover, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." ACS Hospital System, Inc v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The Examiner must point to something in the prior art that suggests in some way a modification of a particular reference or a combination of references in order to arrive at Applicants' claimed invention. Absent such a showing, the Examiner has improperly used Applicants' disclosure as an instruction book on how to reconstruct to the prior art to arrive at Applicants' claimed invention. Furthermore, any deficiencies in the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". See In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002).

In the present situation, since Kardontchik '204 and Yeh '214 fail to disclose or suggest the relationship between "a first loop" and "a second loop" wherein both "said first loop and said second loop are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously" as expressly defined in Applicants' claims 1 and 4, Applicants respectfully request that the rejection of Applicants' base claims 1 and 4 and dependent claim 5 be withdrawn.

Separately, claim 14 has been rejected under 35 U.S.C. §102(e) as being anticipated by Barrett et al., U.S. Patent No. 5,422,911 for reasons stated on page 4 of the Office Action (Paper No. 12). As previously discussed, base claim 14 has

been amended to clarify the relationship between an information processing apparatus for data processing based on a clock frequency and a circuitry connected to the information processing apparatus for enabling the information processing apparatus to render variable "a clock frequency based on a remaining charge of a battery so that said information processing apparatus operates on a frequency commensurate which the remaining charge of said battery." This feature is **not** disclosed or suggested in Barrett '911 or any other prior art references of record. As a result, the rejection of Applicants' claim 14 should be deemed moot. Nevertheless, the Examiner has simply reiterated the same rejection without addressing Applicants' arguments for patentability presented earlier. To the extent that Barrett '911 may still be applicable, Applicants respectfully traverse the rejection for reasons discussed herein below.

Base claim 14 defines an information processing system comprising:

> an information processing apparatus for data processing based on a clock frequency; and
> a circuitry connected to said information processing apparatus, for outputting an internal state,
> wherein said information processing apparatus renders variable a clock frequency based on a remaining charge of a battery so that said information processing apparatus operates on a frequency commensurate which the remaining charge of said battery.

As defined in Applicants' base claim 14, the crystal oscillation frequency, based on the battery residue or the remaining charge on the battery, is frequency-divided so that the reference frequency may be lowered to thereby realize an operating frequency commensurate with the battery residue or the remaining charge in the battery. By virtue of the wise operating range PLL, the oscillation frequency can be changed or varied in a wise range (to a great extent) up to the minimum

frequency commensurate with the battery residue or the remaining charge in the battery.

In contrast to Applicants' base claim 14, Barrett '911 discloses a selective call receiver, as shown in FIG. 1, using a phase lock loop (PLL) frequency synthesizer provided with a number of components, shown in FIG. 4, including a charge pump phase/frequency detector 403, a N counter 404, a voltage-to-current converter 410, a programmable gain current multiplier 412, and a current control variable frequency oscillator 413. According to Barrett '911, N is set in control multiplier 412 and N counter 404 by means of the frequency control signal code from controller so that the frequency signal may be changed programmably. To this end, the oscillation frequency of the internal oscillator 414 in the PLL is changed so as to enable a wide range operation.

However, Barrett '911 does **not** disclose or suggest of how prolonging of the battery life is reflected to the frequency dividing ratio of a clock frequency so that the information processing apparatus can operate on a frequency commensurate with the remaining charge of the battery, as defined in Applicants' base claim 14.

The rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051

(Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

In the present situation, since Barrett '911 fails to disclose or suggest key aspects of Applicants' base claim 14, Applicants respectfully request that the rejection of claim 14 be withdrawn.

Claims 9, 10, 11, 12 and 15-17 have been rejected under 35 U.S.C. §103 as being unpatentable over Barrett, Jr. et al., U.S. Patent No. 5,422,911, in view of Kardontchik et al., U.S. Patent No. 5,566,204 for reasons stated on pages 5-6 of the Office Action (Paper No. 12). Again, Applicants submit that features of Applicants' claims 9, 10, 11, 12, 15 and 16 are **not** disclosed or suggested by Barrett '911 and Kardontchik '204, whether taken individually or in combination with any other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection for the following reasons.

First of all, Applicants note that claims 15-16 depend upon base claim 14, which Applicants have already pointed as patentably distinguishable over Barrett '911 for reasons discussed. As dependent claims, claims 15-16 should be allowed if base claim 14 is allowable.

With regard to claim 9, claim 9 defines an information processing apparatus as comprising:

> a clock generator unit including a first control signal generator unit for generation of a first control signal based on a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal based on a difference in frequency between an input signal and an output signal, and an oscillator for generation of a clock signal based on said first control signal and said second control signal;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock signal as generated by said clock generator unit.

Likewise, claim 11 alternatively defines an information processing apparatus as comprising:

a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input thereto;

a clock control unit for controlling said first clock signal as input to said clock generator unit; and

a logic unit for processing data on the basis of said second clock signal.

As expressly defined in each of Applicants' base claims 9 and 11, the phase locked loop (PLL) circuit is provided with two loops (i.e., first feedback circuit and second feedback circuit) operating continuously.

In contrast to Applicants' base claims 9 and 11, Barrett '911, as a primary reference, only discloses a selective call receiver, as shown in FIG. 1, using a phase lock loop (PLL) frequency synthesizer provided with a number of components, shown in FIG. 4, including a charge pump phase/frequency detector 403, a N counter 404, a voltage-to-current converter 410, a programmable gain current multiplier 412, and a current control variable frequency oscillator 413. Again, Barrett '911 changes the oscillation frequency of an internal oscillator 414 so as to enable a wide range operation.

However, no disclosure of any "clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second

clock signal identical in frequency to said first clock signal being input thereto" as defined in Applicants' base claim 11 and any "clock generator unit including a first control signal generator unit for generation of a first control signal based on a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal based on a difference in frequency between an input signal and an output signal, and an oscillator for generation of a clock signal based on said first control signal and said second control signal" as defined in Applicants' base claim 9.

As a secondary reference, Kardontchik '204 does **not** and can**not** remedy the noted deficiencies of Barrett '911 in order to arrive at Applicants' base claims 9 and 11. This is because Kardontchik '204 only discloses an integrated CMOS circuit as shown in FIG. 2, including a receiver section with a phase-locked loop (PLL) and a transmitter section with a locked loop (LL), wherein the receiver section provides fast clock acquisition of an incoming data signal.

Neither Barrett '911 nor Kardontchik '204 discloses any clock generator unit having two feedback circuits (loops) operating continuously. In fact, in Kardontchik '204, the phase detector and frequency divider are provided and switched by the multiplexer so that only one of them is operating at a time. Likewise, in Barrett '911, the phase/frequency detector 403 is made up of an integrated single circuitry having a single loop.

In view of the foregoing deficiencies of the proposed combination of Barrett '911 and Kardontchik 204, Applicants respectfully request that the rejection of claims 9, 10, 11, 12, 15 and 16 be withdrawn.

Lastly, claim 13 has been rejected under 35 U.S.C. §103(b) as being unpatentable over **newly cited art**, Ooishi et al., U.S. Patent No. 5,783,956, in view of Kardontchik et al., U.S. Patent No. 5,566,204, for reasons stated on pages 6-7 of the non-final Office Action (Paper No. 12). Specifically, the Examiner asserts that Ooishi '956 discloses all aspects of Applicants' claim 13, except for "the first and second feedback loops for controlling the phase and frequency of the oscillator" which is allegedly disclosed by Kardontchik '204, see FIG. 1. Again, the Examiner's assertion is factually incorrect, primarily because Kardontchik '204 does not disclose the use of "the first and second feedback loops for controlling the phase and frequency of the oscillator" as alleged by the Examiner. Moreover, Applicants further traverse the rejection for reasons discussed herein below.

Base claim 13 defines an information processor apparatus comprising:

> a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input;
>
> a plurality of circuits operable based on said second clock signal as output from said clock generator unit; and
>
> an interface for transmission of said second clock signal to more than one circuit selected from among said plurality of circuits being operable with a power supply different from that of said clock generator unit.

As defined in Applicants' base claim 13, the information processing apparatus includes a PLL, a processor and so on disposed on the same IC having different regions, (for example, one operating on 3.3. volts and another operating on 1.8 volts), and the wise operating range PLL can be used regardless of which of the regions the PLL is placed without altering the circuit constitution or configuration. As a result, the PLL can be used without paying attention to the power supply voltage

used, as described on page 36, line 27 extending to page 38, line 20 of Applicants' original specification.

In contrast to Applicants' base claim 13, Ooishi '956 addresses a different set of problems, one that is in a built-in PLL of a semiconductor device (SRAM), in which the oscillation frequency of a ring oscillator in the PLL easily fluctuates due to fluctuation in the power supply potential, thereby making it difficult to lock the internal clock in the external clock, see col. 4, lines 40-49.

The purpose of Ooishi '956 is to stabilize the power supply potential for PLL and SRAM by providing a converter within the semiconductor device. To this end, Ooishi '956 provides on the IC, a series-type converter for generating a stable 3 volts from external 5 volt power supply so that the stable converter output voltage can be used as the power supply of the PLL and SRAM. According to Ooishi '956, the PLL and SRAM are operated on the same voltage or potential and the use of the built-in power supply is for the sake of stabilized PLL control. Although on the IC are the region of PLL and SRAM and the region of the internal power supply for converting 5 volts to 3 volts, such provision of the separate regions is different from separating the PLL region and the SRAM region in purpose.

In contrast to the converter within IC for the purpose of stabilized PLL operation as disclosed by Ooishi '956, Applicants' base claim 13 is directed to a PLL scheme which can be used in either of 3.3. volt region or 1.8 volt region on the same IC without modifying circuit configuration. As a result, Applicants' base claim 13 and Ooishi '956 are different in purpose as well as configuration.

As a secondary reference, Kardontchik '204 does **not** and can**not** remedy the noted deficiencies of Ooishi '956 in order to arrive at Applicants' base claim 13. This

is because Kardontchik '204 does not disclose the use of the "first and second feedback circuits for controlling the phase and frequency of the oscillator" as alleged by the Examiner.

In view of the foregoing deficiencies of the proposed combination of Ooishi '956 and Kardontchik 204, Applicants respectfully request that the rejection of Applicants' base claim 13 be withdrawn.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600. Applicants respectfully reserve all rights to file subsequent related application(s) (including reissue applications) directed to any or all previously claimed limitations/features which have been amended or canceled, or to any or all limitations/features not yet claimed, i.e., Applicants have no intention or desire to dedicate or surrender any limitations/features of the disclosed invention to the public.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned

attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 500.38017X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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